IN THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Currently amended) A system for converting an input voltage VIN to a digital

output, comprising: K linear flash-type analog-to-digital (A/D) converter apparatuses Z1, Z2, . . . , ZK respectively characterized by reference voltage step sizes ΔV1, ΔV2, . . . , ΔVK and respectively adapted to convert VIN into multibit strings S1, S2, . . . , SK, wherein ΔV1<ΔV2< . . . <ΔVK, and wherein K is greater than or equal to 2; and encoder means for applying ~~a scale factor to~~multiplying or dividing at least a selected one of S1, S2, . . . , and SK by a value to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within S1, S2, . . . , and SK.

16. (Previously presented) The system of claim 15, wherein S1, S2, . . . , and SK each have a same number of bits.

17. (Previously presented) The system of claim 15, wherein S1, S2, . . . , and SK do not each have a same number of bits.

18. (Previously presented) The system of claim 15, wherein for k-1, 2, . . . , K the A/D converter apparatus Zk comprises an arithmetic unit Ak in series with an A/D converter Bk, wherein the A/D converters have a same working voltage range, wherein VIN is within the working voltage range, wherein the working voltage range comprises K contiguous voltage subranges denoted as δV1, δV2, . . . , δVK in order of lower to higher voltages, wherein for k=1, 2, . . . , K the arithmetic unit Ak is adapted to change VIN into a new input voltage VIN,k in accordance with a transformation of δVk into the working voltage range and A/D converter Bk is adapted to transform VIN,k into the multibit string Sk.

19. (Previously presented) The system of claim 18, wherein δV1, δV2, . . . , δVK have values such the error of the digital output relative to VIN is a piecewise continuous function of VIN within the working voltage range, said piecewise continuous function of VIN, the piecewise continuous function having K pieces, wherein the relative error within each said piece of the K pieces is a monotonically decreasing function of VIN, and wherein each piece of the K pieces has about a same maximum relative error.

20. (Previously presented) The system of claim 15, wherein K=2, wherein the A/D converter apparatuses Z1 and Z2 comprise A/D converters B1 and B2 having working voltage ranges δ1 and δ2, respectively, such that δ2 is a subset of δ1 and δ2/δ1 is an integer subject to δ2/δ1>1, wherein B1 and B2 are respectively adapted to convert VIN to S1 and S2, and wherein the encoder means is adapted to generate the digital output as S2 if S2 is not within the voltage range δ1 else the encoder means is adapted to generate the digital output as S1 multiplied by δ2/δ1.

21. (Previously presented) The system of claim 20, wherein δ2/δ1=2J, and wherein J is a positive integer.

22. (Currently amended) A method for converting an input voltage VIN to a digital output, comprising: providing K linear flash-type analog-to-digital (A/D) converter apparatuses Z1, Z2, . . . , ZK respectively characterized by reference voltage step sizes ΔV1, ΔV2, . . . , ΔVK, wherein ΔV1<,ΔV2< . . . <ΔVK, and wherein K is greater than or equal to 2; converting VIN, by converter apparatuses Z1, Z2, . . . , ZK, into multibit strings S1, S2, . . . , SK, respectively; and <u>multiplying or dividing at least a selected one of</u>~~combining~~ S1, S2, . . . , and SK <u>by a value</u> to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within S1, S2, . . . , and SK.

23. (Previously presented) The system of claim 22, wherein S1, S2, . . . , and SK each have a same number of bits.

24. (Previously presented) The method of claim 22, wherein S1, S2, . . . , and SK do not each have a same number of bits.

25. (Previously presented) The method of claim 22, wherein for k=1, 2, . . . , K the A/D converter apparatus Zk comprises an arithmetic unit Ak in series with an A/D converter Bk, wherein the A/D converters have a same working voltage range, wherein VIN is

within the working voltage range, wherein the working voltage range comprises K contiguous voltage subranges denoted as $\delta V1, \delta V2, \ldots, \delta VK$ in order of lower to higher voltages, said method further comprising: changing VIN by the arithmetic unit Ak for $k=1, 2, \ldots, K$, into a new input voltage VIN,k in accordance with a transformation of δVk into the working voltage range; and transforming VIN,k by the A/D converter Bk, into the multibit string Sk.

26. (Previously presented) The method of claim 25, wherein $\delta V1, \delta V2, \ldots, \delta VK$ have values such the error of the digital output relative to VIN is a piecewise continuous function of VIN within the working voltage range, said piecewise continuous function of VIN, the piecewise continuous function having K pieces, wherein each two consecutive pieces of the K pieces are discontinuously joined together, wherein the relative error within each said piece of the K pieces is a monotonically decreasing function of VIN, and wherein each piece of the K pieces has about a same maximum relative error.

27. (Previously presented) The method of claim 22, wherein K=2, wherein the A/D converter apparatuses Z1 and Z2 comprise A/D converters B1 and B2 having working voltage ranges $\Delta 1$ and $\Delta 2$, respectively, such that $\delta 2$ is a subset of $\delta 1$ and $\delta 2/\delta 1$ is an integer subject to $\delta 2/\delta 1>1$, wherein B1 and B2 are respectively adapted to convert VIN to S1 and S2, and wherein said combining includes generating the digital output as essentially S2 if S2 is not within the voltage range $\delta 1$ else said combining includes generating the digital output essentially as S1 multiplied by $\delta 2/\delta 1$.

28. (Previously presented) The method of claim 27, wherein $\delta 2/\delta 1=2J$, and wherein J is a positive integer.